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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/964,865	09/28/2001	Patrik Eriksson	2380-348	2363

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EXAMINER	
RAMAKRISHNAIAH, MELUR	
ART UNIT	**PAPER NUMBER**
2643	

DATE MAILED: 11/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/964,865	ERIKSSON ET AL.	
	Examiner	Art Unit	
	Melur Ramakrishnaiah	2643	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 September 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-44* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13,16-36 and 39-44* is/are rejected.

7)☒ Claim(s) *14,15,37 and 38* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *9-28-01/4-10-02*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-10, are rejected under 35 U.S.C 102(e) as being anticipated by Amrany et al. (US PAT: 6,597,746, filed 2-17-2000, hereinafter Amrany).

Regarding claims 1, Amrany discloses a method for reducing a peak-to average ratio (PAR) of a signal comprising: receiving a input signal (fig. 6), generating an offset signal in (302, fig. 6) associated with the input signal, combining the input signal and the offsetting signal so that offsetting signal reduces the PAR of the input signal to produce a combined signal, processing the combined signal and the offsetting signal, and combining the processed combined signal and the processed offsetting signal (figs. 4-6, col. 9, line 45 – col. 10, line 34).

Regarding claims 2-10, Amrany teaches the following: input signal is a multi-carrier signal, offsetting signal (reads on 302) is an anti-phase signal, processing includes converting the combined signal and the offsetting signal from the digital form into a analog form and analog combined signal and the analog offsetting signal are combined in step to generate an analog combined signal, transmitting the analog combined signal, performing analog processing at (206, fig. 6) on the analog combined

signal before transmission, processing includes analog processing the combined signal and the offsetting signal before combining and transmission, offsetting signal is converted to analog signal form using plural digital-to-analog converters (like 206, fig. 6), combined signal and offsetting signal are each converted into analog form using respective digital-to-analog converters (like 206, fig. 6) and wherein each digital-to-analog converter has substantially the same/different characteristics (this is implicit in as much as the characteristics of them depends on the signal levels; figs. 4-6, col. 9, line 45 – col. 10, line 34).

3. Claims 11-13, 16-21, 22-25, 26-33, 34-36, 39-44 are rejected under 35 U.S.C 102(e) as being anticipated by Hunton (US 2003/0026351 A1, Provisional application No. 60/309,571, filed on Aug. 2, 2001).

Regarding claim 11, Hunton discloses a method for reducing a peak-to average ratio (PAR) of a signal comprising: receiving a digital input signal, formulating the anti-phase signal for the input signal at (110, figs. 2-3), combining the input signal and anti-phase signal to produce a peak limited digital signal, converting the peak limited signal in a first digital-to-analog converter (reads on 30) into a peak-limited analog signal, converting the anti-phase digital signal in a second digital analog converter (reads on 30) into an anti-phase analog signal and combining the peak limited and ant phase signal to produce a combined signal (paragraphs: 0022 – 0026).

Regarding claim 22, Hunton discloses a method, comprising: reducing in a digital domain a a peak-to average ratio (PAR) of a signal having an initial PAR, converting the

reduced PAR digital signal into the analog domain to provide a reduced PAR signal, and removing the distortion in the reduced PAR analog signal caused by PAR reducing step in the analog domain (figs. 2-3, paragraphs: 0022 – 0026).

Regarding claim 26, Hunton discloses an apparatus for reducing peak-to average ratio (PAR) of a signal comprising: first electronic circuitry (110, figs. 2-3) configured to generate an offsetting signal associated with the input signal, a first combiner (130, fig. 3) configured to combine the input signal and the offsetting signal so that offsetting signal reduces the PAR of the input signal to produce a combined signal, a second electronic circuitry (reads on 40, fig. 2) configured to process the combined signal and the offsetting signal, second combiner configured to combine the processed signal and the processed offsetting signal (figs. 2-3, paragraphs: 0022 – 0026).

Regarding claim 34, Hunton discloses an apparatus for reducing peak-to average ratio (PAR) of a signal comprising: first electronic circuitry (110, figs. 2-3) to receive a digital input signal and to formulate an anti-phase signal for the input signal, a first combiner (130, fig. 3) configured to combine the input and anti-phase signal to produce a peak-limited digital signal, a first digital-to- analog converter (for example 30, fig. 2) to convert peak-limited digital signal into a peak-limited analog signal, a second digital-to-analog converter (like 30, fig. 2) convert configured to convert the anti phase digital signal to anti-phase analog signal, and a second combiner (reads on 40, fig. 2) configure to combine the peak-limited analog signal and the anti-phase analog signal (figs. 2-3, paragraphs: 0022 – 0026).

Regarding claims 12-13, 16-21, 23-25, 27-33, 35-36, 39-44, Hunton further teaches the following: changing the a sign of the anti-phase signal or inverting the antiphse signal before combining peak-limited and anti-phase analog signals, anti-phase signal limits the input signal peak to a threshold associated with a range of the first digital-to- analog converter (this is implicit as D/A is processing peak limited signal), combining removes distortion caused by peak-limiting the input signal, transmitting the combined analog signal, performing analog processing on the combined analog signal before transmission, analog processing the peak limited analog signal and the anti-phase analog signal before the combining and transmission, first and second digital-to- analog converter (30, fig. 2) have substantially the same/different characteristics (this is implicit in as much as the characteristics of them depends on the signal levels), removing step includes restoring the initial PAR from the reduced PAR analog signal, PAR reducing step is accomplished by an anti-phase signal to offset peaks of the signal in digital domain, transforming the anti-phase signal into an in-phase signal, converting the in-phase analog signal into the analog domain, and wherein restoring step includes combining the analog in phase signal with the reduced PAR analog signal, input signal is a multi-carrier signal (fig. 2), offsetting setting signal is an anti-phase signal, second electronic circuitry includes first and second digital-to- analog converters (30, fig. 2) for converting the combined signal and the offsetting signal, respectively into analog form, and the second combiner (reads on 40, fig. 2) is configured to combine the analog combined signal and analog offsetting signal to generate an analog combined signal, third electronic circuitry (50, fig. 2) configured to process combined before transmission,

third electronic circuitry configured to process in the analog domain the combined signal and offsetting signal before combining, combining the input and anti-phase signal limits the input signal peak value to a threshold associated with a range of the first digital-to-analog converter, a third digital-to-analog converter (like 30, fig. 2) configured to convert the anti-phase signal into an anti-phase analog signal, wherein first electronic circuitry is configured to map the anti-phase signal to the second signal and third digital-to-analog converters and to the first combiner (130, fig. 3), and wherein the second and third digital-to-analog converter provide corresponding outputs to the second combiner (reads on 40,figs. 2-3, paragraphs: 0022 – 0026).

4. Claims 14-15, 37-38 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Melur Ramakrishnaiah whose telephone number is (571)272-8098. The examiner can normally be reached on 9 Hr schedule.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Curt Kuntz can be reached on (571) 272-7499. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Melur Ramakrishnaiah
Primary Examiner
Art Unit 2643